

# CMOS-Compatible RF-MEMS Tunable Capacitors

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**Abstract** — New CMOS-MEMS tunable capacitors have been designed, fabricated and tested. Large-tuning range and high quality factor,  $Q$ , are achieved. The structures were made from the CMOS interconnect stack using a maskless CMOS micromachining process. Our tunable capacitor designs can be classified into two categories based on their tuning schemes as gap&area tuning and gap-only tuning. The capacitors with gap&area tuning were fabricated using Austria Microsystems (AMS) 0.6  $\mu\text{m}$  and Agilent 0.5  $\mu\text{m}$  CMOS processes. These devices have a measured nominal capacitance of 209 fF and a measured  $Q$  of 28 at 1.5 GHz. The capacitance change is measured from 209 fF to 294 fF within a 24 V control voltage, and 72.4 mW power at 1.5 GHz. The capacitors with gap-only tuning were fabricated in the TSMC 0.35  $\mu\text{m}$  CMOS process and have larger tuning range and more power efficiency than the 1st generation designs. For these new designs, 3.52 to 1 tuning range has been measured with tuning from 42 fF to 148 fF within a 12 V control voltage and 34mW power and  $Q$  of 52 at 1.5 GHz. The tuning mechanism uses electro-thermal actuation. The essential differences between this work and prior work are the CMOS compatibility and more area efficiency at several gigahertz. Wide-range VCOs can be designed by using these MEMS tunable capacitors, inductors and CMOS or SiGe electronics on the same chip. Parasitic losses can be minimized and phase noise performance can be improved.

## I. INTRODUCTION

There is a continuing demand to integrate complete systems on a single integrated circuit. These systems require voltage-controlled oscillators (VCOs) with gigahertz frequencies, and low phase noise. High- $Q$  tunable capacitors are desired by VCOs for better phase noise performance. Micro-mechanical tunable capacitors have been used for getting high- $Q$  for VCO applications [1-2]. In the past few years, tunable capacitors based on MEMS technology have been designed [1-4], with tuning range in excess of 840% [3]. Several other strategies, which include the implementation of MOS varactors or switched capacitor banks, have been used to achieve wide tuning range. Distortion and linearity are the two main problems associated with these approaches. Compared with solid-state varactors, MEMS tunable lower

capacitors have advantages of lower loss, larger tuning range and more linear tuning characteristic.

In this paper, new CMOS-compatible micromechanical tunable capacitors are demonstrated. Using new design features, tuning ratios over 353% have been achieved, while still maintaining a  $Q$  above 50 at 1.5GHz. Previous designs use separately fabricated CMOS electronics for potential applications like VCOs [1-3], as the capacitors are not integrated with the transistors. In our present work, the structures are made using the CMOS interconnect stack and released with a maskless CMOS micromachining process [5]. A key advantage of this approach is that CMOS electronics for VCOs and other possible applications are integrated on the same chip. Losses coming from the interconnect between chips in multi-chip solutions are eliminated, resulting in lower phase noise and higher signal levels.

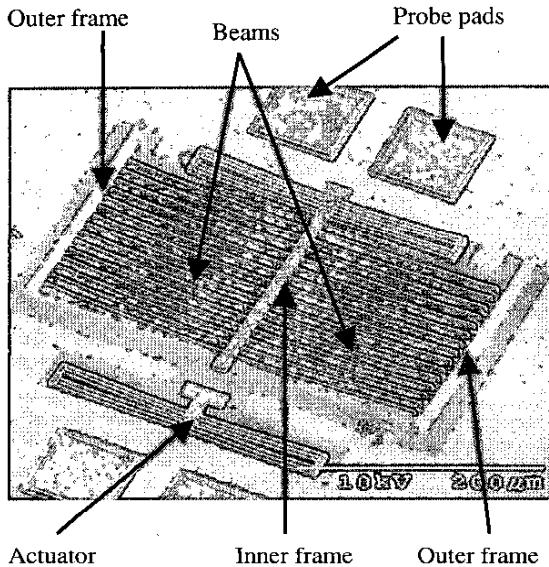
Previous VCO designs with micromechanical tunable capacitors have not achieved wide tuning for VCO application. Off-chip interconnects introduce fixed capacitance to LC tank of the VCO, which decrease the tuning range for the VCO [1]. The new tunable capacitors can be used in wide-tuning-range VCOs, having less parasitic capacitance.

## II. DESIGN AND FABRICATION

The high-aspect-ratio CMOS micromachining technology [5] begins with a conventional foundry CMOS process. Versions of these actuators were fabricated using Austria Microsystems (AMS) 0.6  $\mu\text{m}$  CMOS, Agilent 0.5  $\mu\text{m}$  CMOS and TSMC 0.35  $\mu\text{m}$  CMOS. After the foundry fabrication, several etch steps are used to release the structure. The undercut of silicon in the release step requires the placement of active circuits to be at least 40  $\mu\text{m}$  away from the released MEMS structures. Our tunable capacitor designs can be classified into two categories based on their tuning schemes. Both gap and area tuning are used for 1<sup>st</sup> generation capacitors, and gap-only tuning is used for the 2<sup>nd</sup> generation capacitors.

### A. Tunable Capacitor Designs using Gap & Area Tuning (1<sup>st</sup> Generation Tunable Capacitors)

Tunable capacitors using gap & area tuning were fabricated using AMS 0.6  $\mu\text{m}$  and Agilent 0.5  $\mu\text{m}$  CMOS process. Electro-thermal actuators are used for the MEMS tunable capacitor design (Fig. 1). In contrast, some previous works used electrostatic actuators [1-2]. Polysilicon resistors act as heaters inside the inner frame. Upon heating the structure, the interdigitated beams curl down vertically and also curl sideways. This curling changes the area between interdigitated beams for tuning. The reason of this curling behavior is that metal and oxide layers inside the beams have different TCE values. Gap tuning is achieved by electro-thermal actuators, which were presented in [6].

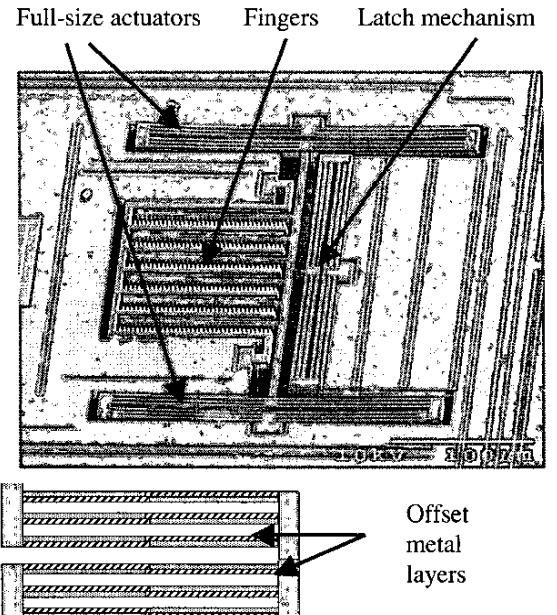


**Figure 1.** Scanning electron micrograph (SEM) of a released tunable capacitor in the Agilent 0.5  $\mu\text{m}$  CMOS process.

### B. Tunable Capacitor Designs using Only Gap Tuning (2<sup>nd</sup> Generation Tunable Capacitors)

These capacitors were fabricated using TSMC 0.35  $\mu\text{m}$  CMOS process. Gap tuning is again achieved by electro-thermal actuators. Instead of interdigitated beams, small comb fingers are used to increase the tuning range and area efficiency. Fig. 2(a) shows a 2<sup>nd</sup> generation released tunable MEMS capacitor with full-size actuators. One of the design goals was switching between multiple capacitors with low power operation. For these designs, lateral electro-thermal actuators are used for implementation of lateral latch structures. By using these latch structures, we intended to consume power only when switching between fixed capacitance values. The latch structures in the TSMC 0.35  $\mu\text{m}$  chip did not work, as the actuators did not displace upon release. The microstructures in this process had lower stress gradients than anticipated, based on our experience with other CMOS processes. Future latch designs will consume

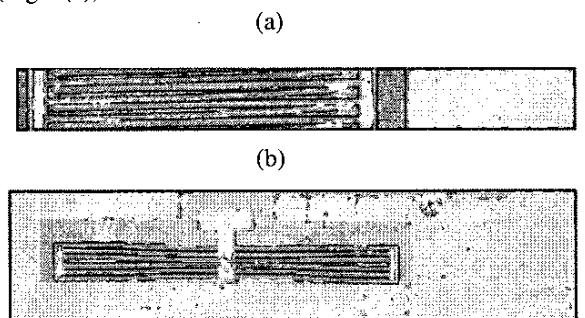
no power when operating statically at one fixed capacitance value. Half-size electro-thermal actuators in TSMC 0.35  $\mu\text{m}$  CMOS process with a length of 124  $\mu\text{m}$  and a width of 22  $\mu\text{m}$  give measured actuation of 5.5  $\mu\text{m}$  with 8.4 mW of heating power (Fig. 2(b)). The lateral stress gradient arises from purposefully offsetting the lower metal layers with respect to the top metal layer of a CMOS-MEMS beam [6].



**Figure 2.** (a) SEM of a released capacitor in the TSMC 0.35  $\mu\text{m}$  CMOS process with full-size actuators. (b) half-size actuator layout.

### III. MEASUREMENT RESULTS

The summary of the experimental tunable capacitors and their measured capacitances, power and Q values are shown in Table I.  $S_{11}$  parameters of the 1<sup>st</sup> and 2<sup>nd</sup> generation tunable capacitors are measured using an Agilent E8364A network analyzer from 45MHz to 3GHz. The 1<sup>st</sup> generation designs have low tuning ratios compared to the 2<sup>nd</sup> generation designs. The reason for this low tuning range in AMS 0.6  $\mu\text{m}$  CMOS process is the excessive lateral beam curling, which causes the fingers to snap together. The fingers stick in their positions, and can't be used for tuning (Fig. 3(a)).



**Figure 3.** Lateral curling from stress gradients. (a) Interdigitated beams in the AMS 0.6  $\mu\text{m}$  CMOS process, and (b) electrothermal actuator in the Agilent 0.5  $\mu\text{m}$  CMOS process.

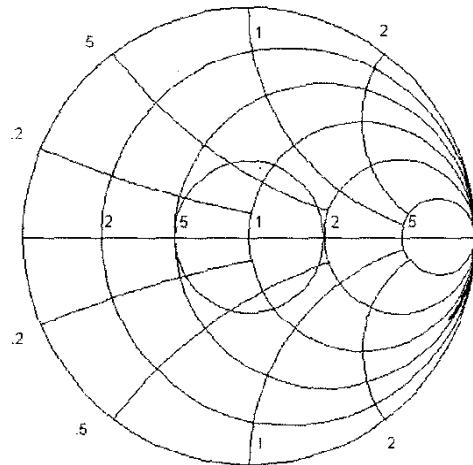
TABLE I  
CHARACTERISTICS OF CMOS-MEMS TUNABLE CAPACITORS

Device	Overall size( $\mu\text{m} \times \mu\text{m}$ )	$C_{\text{MIN}}$ (fF)	$C_{\text{MAX}}$ (fF)	Tuning Range	$V_{\text{TUNE}}$ (V)	Power (mW)	Q at 1.5GHz
1 <sup>st</sup> generation design in AMS process	170×220	153	175	14.4%	12	25.5	24
1 <sup>st</sup> generation design in Agilent process	230×270	209	284	35.9%	24	72.4	28
TSMC design with full actuator	228×250	42	148	352.4%	12	34.2	52
Compact TSMC design with full actuator	228×230	40	98	245%	12	27.1	40
TSMC design with half actuator	150×250	53	108	203.8%	6	22.4	35
Compact TSMC design with half actuator	150×230	35	102	291.4%	6	18.3	48

The reason for low tuning range in the devices fabricated with the Agilent 0.5 $\mu$ m CMOS process is that electro-thermal actuators displaced in an opposite way of the intended direction upon release (Fig. 3(b)). This observation underscores that each CMOS process is different and must be completely characterized. For 2<sup>nd</sup> generation capacitors, large tuning ratios have been achieved, by using the comb finger gap-only tuning mechanism, instead of the interdigitated beam gap & area tuning. These 2<sup>nd</sup> generation capacitor designs have also higher Q values and less power consumption compared to 1<sup>st</sup> generation chips.

## *A. RF Characterization of the 1<sup>st</sup> Generation Designs in Agilent 0.5 $\mu$ m CMOS Process*

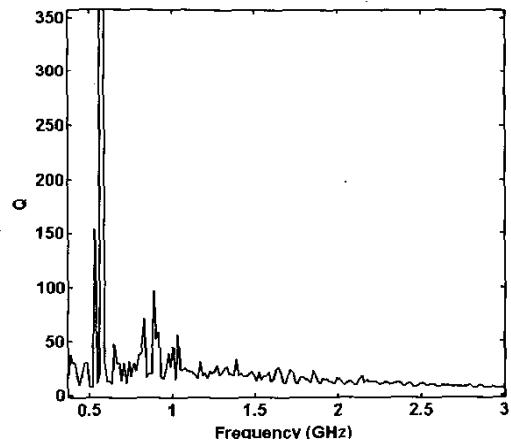
Measured  $S_{11}$  parameters of the 1<sup>st</sup> generation design in the Agilent 0.5  $\mu$ m CMOS process is shown in Fig. 4. Measured Q values at minimum capacitance versus frequency are shown in Fig. 5. The device has a Q above 38 up to 1 GHz.



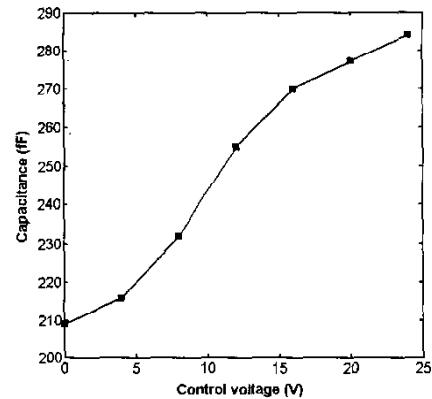
**Figure 4.** Measured S11 plot of the 1<sup>st</sup> generation tunable capacitor designs in Agilent 0.5  $\mu$ m CMOS process.

The measured tuning characteristic at a fixed frequency of 1.5 GHz does not exhibit linear tuning. The reason for this problem may be capacitance changes nearby the device. Nearby tuning capacitor designs were observed to also actuate slightly during thermal actuation of the device. The

device under test must better thermally isolated to completely isolate it from the surrounding structures.



**Figure 5.** Measured quality factor of the 1<sup>st</sup> generation tunable capacitor designs in Agilent 0.5  $\mu$ m CMOS process from 400 MHz to 3GHz.



**Figure 6.** Measured tuning characteristic of the 1<sup>st</sup> generation tunable capacitor designs in Agilent 0.5  $\mu$ m CMOS process.

### *B. RF Characterization of the 2nd Generation Designs in TSMC 0.35 $\mu$ m CMOS Process*

The RF characteristic were measured for the compact TSMC design with a half actuator shown in Fig. 7. Q values and the tuning characteristic for the 2<sup>nd</sup> generation tunable capacitor designs in the TSMC 0.35  $\mu$ m CMOS process are shown in Fig. 8 and Fig. 9, respectively. The compact design

in Fig. 7 has four groups with 36 fingers and 71 gaps. A second TSMC design has six groups of 36 fingers. The calculated capacitance for 0V control voltage is 58fF. For

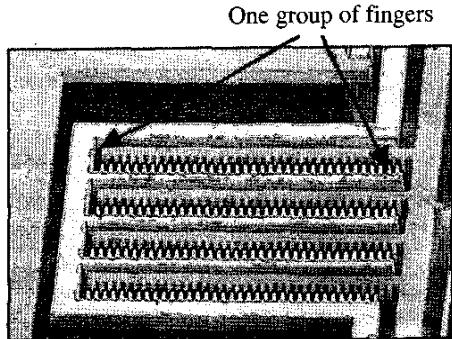


Figure 7. SEM of the compact TSMC 0.35  $\mu$ m CMOS process. design with half actuator.

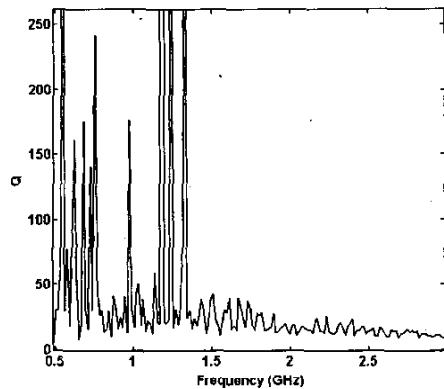


Figure 8. Measured quality factor of the 2<sup>nd</sup> generation tunable capacitor designs in the TSMC 0.35  $\mu$ m CMOS process from 400 MHz to 3GHz.

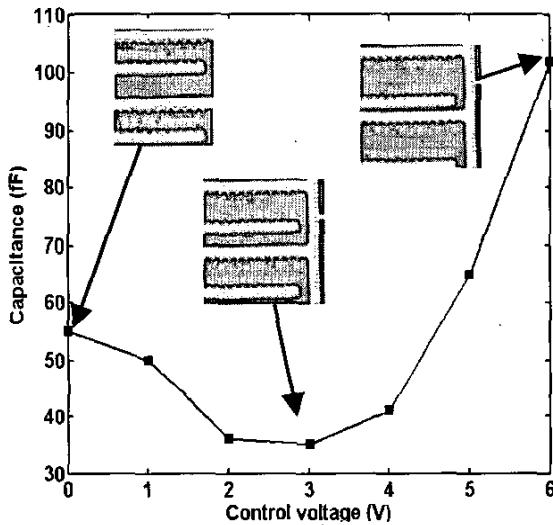


Figure 9. Measured tuning characteristic of the 2<sup>nd</sup> generation tunable capacitor designs in the TSMC 0.35  $\mu$ m CMOS process.

this calculation, the estimated gap of 0.6  $\mu$ m between fingers is used. The metal stack thickness is assumed as 7  $\mu$ m and the maximum overlap between fingers is taken as 2  $\mu$ m for calculations. The calculated 58fF value is really close to measured value, which is 55fF. The calculated capacitance for 6V control voltage is 124fF, which is also close to measured value of 102fF. In Fig. 9, three small pictures are showing the location of finger groups for different control voltages. The 2<sup>nd</sup> generation tunable capacitor has a Q above 20 up to 2.7 GHz making it suitable for higher frequency applications.

#### IV. CONCLUSIONS

A new CMOS-compatible RF-MEMS tunable capacitor has been designed, fabricated and tested by using AMS 0.6  $\mu$ m, Agilent 0.5  $\mu$ m and TSMC 0.35  $\mu$ m CMOS processes. The essential differences between this work and prior work are the CMOS compatibility and using a maskless CMOS micromachining process. The 2<sup>nd</sup>-generation tunable capacitor achieves large tuning range up to 352.4% and Q up to 52 at 1.5 GHz. For future work, the latch mechanism for low power design will be implemented and the design to make more overlap between fingers will be investigated. These efforts will lead to eventual optimization of the tuning range and area efficiency.

#### ACKNOWLEDGEMENT

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